CLAIMS:

1. An apparatus for testing an integrated circuit (10), the apparatus comprising:

- a compactor (22) to compress test responses from a circuit-under-test (14) that is part of an integrated circuit 10; and

- masking circuitry (18) coupled between the circuit-under-test and the compactor (22) for masking one or more of the test responses from the circuit-under-test (14), characterized in that the masking circuitry (18) further comprises decompression circuitry (26, 30, 36, 38) for receiving compressed mask data (m_1-m_q) from the apparatus and providing decompressed mask data to the mask circuitry (40).

2. An apparatus as claimed in claim 1 wherein decompression is performed by a linear-feedback shift register (26).

3. An apparatus as claimed in any of the preceding claims wherein decompression is performed by phase shifter (30).

4. An apparatus as claimed in any of the preceding claims wherein decompression is performed by weighting logic.

5. An apparatus as claimed in any of the preceding claims wherein, the compressed mask data comprises at least one control signal for controlling the masking circuitry (18).

6. An apparatus as claimed in claim 5 wherein, the at least one control signal is a mask all control signal.

7. An apparatus as claimed in claim 5 wherein, the at least one control signal is a mask enable control signal.

8. A method used in the testing of an integrated circuit (10), characterized by comprising the steps of:

- providing compressed mask data to decompression circuitry;
- decompressing the compressed mask data to produce decompressed mask data; and
- masking test responses from the integrated circuit (10) in response to the decompressed mask data.

9. A method for computing compressed mask data for use in masking test data from an integrated circuit (10), characterized in that it comprises the steps of:

- generating a set of equations associated with the mask data; and
- solving the equations to obtain compressed mask data.